REMARKS/ARGUMENTS

The office action mailed on February 24, 2011, has been reviewed and carefully considered. Reconsideration is respectfully requested.

Amendments to the Claims

Claims 1, 3, 6 and 7 remain pending in the present application prior to this amendment. Claims 1, 3, 6 and 7 have been amended. The amendments are self-explanatory and do not introduce new matter.

Claim Objections

In the office action (page 2), claim 3 stands objected to as containing informalities. Applicant has amended claim 3 to replace "first programming or erasing instructions" with --first programming or erasing instruction-- as suggested in the Office action. Withdrawal of the objection is therefore respectfully requested.

Claim Rejections - 35 U.S.C. §103

In the office action (page 2), claims 1, 3, 6 and 7 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Publication No. 2005/0010717 (Ng) in view of U.S. Patent No. 6,081,878 (Estakhri).

Claim 1 has been amended to make the subject matter of claim 1 more clear. Applicant respectfully submits that the amended claim 1 is patentable over *Ng* in view of *Estakhri et al.* at least for the following reasons.

Ng discloses an interleaving method for accessing flash memory cells using double parallel tracks. According to *Ng*, the blocks in two flash memory cells are partitioned to odd logical block addresses and even logical block addresses. To read from two flash memory cells (as shown in Fig. 4A) or to write data into the two flash memory cells (as shown in Fig. 4B), the controller in *Ng* takes two pages at a time to begin the reading/writing proceeding at a time. In particular, *Ng* proceeds the reading/writing according to the odd or even address (steps 310~340). However, *Ng* refers to just one

flash chip. In addition, it is required that two sets of independent USB ports connect to the two flash memory cells separately.

In contrast, according to the independent claim 1 of the present application, the physical blocks in at least two flash chips are partitioned to odd logical block addresses and even logical block addresses, respectively; during the writing/ reading, the flash chip is selected according to the parity of the logical block address. In addition, there is no need to set up two or more sets of independent USB ports for transferring the data. That is, the reading/writing may be simultaneously carried out between/in at least two flash chips and this Multi-Channel mode in at least two flash chips is different from the interleaving mode in one flash chip as disclosed in *Ng*.

As to *Estakhr et al.*, although they disclose a method for increasing the memory performance of flash memory devices by simultaneously writing sectors in multiple flash memory devices, such as, the flash chips 670 and 672 (column 6, lines 23-52). In the OA, the examiner asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to have used a flash memory comprising at least two chips and a controller as described by *Estakhr et al.* in the invention of *Ng* because *Estakhr et al.* shows it is a conventional flash memory (Fig. similar to Fig. 6) and that interleaving may be accomplished in such a setting (Fig. 13).

First of all, it is the fact that *Estakhr et al.* disclose two flash chips 670 and 672, but as the examiner indicates, Fig. 13 of *Estakhr et al.* just shows an interleaving method for accessing the flash memory, which is the same as *Ng*. On the contrary, as mentioned in the above, claim 1 of the present application refers to a Multi-Channel mode for accessing. It is impossible to combine the two interleaving methods in *Ng* and *Estakhr et al.* to obtain the Multi-Channel mode for accessing as claimed in claim 1 of the present application.

Secondly, as is illustrated in Figs. 7, 10, 11 and 13 of *Estakhr et al.*, all of the sectors in one of the flash chips are assigned to odd addresses, while all sectors in the other flash chip are assigned to even addresses. The data in the same row of the sectors is incorporated into one row of data. **It is required 16-bit bus** to reading from or

writing data into the two flash chips 670 and 672, as is illustrated in Fig. 9 of *Estakhr et al*. On the contrary, according to the amended claim 1 of the present application, physical blocks in at least two flash chips are partitioned to odd logical block addresses and even logical block addresses, respectively; during the writing/ reading, the flash chip is selected from the flash chips according to the parity of the logical block address. Accordingly, **it is only required 8-bit reading/writing commands.**

In addition, *Estakhr et al.* adapts such a method that simultaneously reads from or writes into both of the chips by using one instruction as shown in Fig. 9. On the contrary, the present application may use two separate instructions to carry out the reading or writing operation, respectively. After the first instructions for writing the date into one chip have been sent out, the second writing instructions may be sent to the other chip when the signal line of the one chip is BUSY. That is, claim 1 of the present application may access the two chips orderly or in sequence, which is totally different from the simultaneous method of *Estakhr et al.*.

In view of the above mentioned differences, *arguendo*, even if the solution regarding the two chips of *Estakhr et al.* is applied to *Ng*, it cannot obtain the solution as claimed in claim 1 of the present application. Therefore, Applicant respectfully submits that, it is not obvious for those skilled in the art to incorporate the solution regarding the two chips of *Estakhr et al.* into *Ng* to obtain the solutions as claimed in the amended claim 1 of the present application. Accordingly, claim 1 is not obvious in view of *Ng* and *Estakhr et al.* In addition, claims 3, 6 and 7 are patentable over *Ng* in view of *Estakhr et al.*, too, at least because they depend on claim 1 and recite all the limitations of claim 1. Withdrawal of the rejection of claims 1, 3, 6 and 7 under 35 U.S.C. § 103 is respectfully requested.

NO DISCLAIMERS OR DISAVOWALS

Although the present communication may include alterations to the application or claims, or characterizations of claim scope or referenced art, Applicant is not conceding in this application that previously pending claims are not patentable over the cited

references. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Conclusion

For the reasons set forth above, Applicant respectfully submits that claims 1, 3, 6 and 7 pending in this application are in condition for allowance over the cited references. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections and earnestly solicits an indication of allowable subject matter.

This amendment is considered to be responsive to all points raised in the office action. Should the examiner have any remaining questions or concerns, the examiner is encouraged to contact the undersigned attorney by telephone to expeditiously resolve those concerns.

Respectfully submitted,

Dated: May 23, 2011

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